IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Michael G. Kelly and Ravindhar K. Kaw
Title:	**INTEGRATED CIRCUIT INCORPORATING FLIP CHIP AND WIRE BONDING**
Serial No.:	10/678,495
Filing Date:	3 October 2003
Examiner/Unit:	Nitin Parekh / 2811
Attorney Docket No.:	10030203-1 (2116-023-03)

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SEP 1 8 2006
PATENT & TRADEMARK OFFICE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited in the United States Postal Service as First Class Mail in an envelope addressed to:

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on this 14th day of September 2006.

Kelly Pedersen
Signature

DECLARATION PURSUANT TO 37 C.F.R. § 1.131

TO THE COMMISSIONER FOR PATENTS:

This declaration establishes the inventors' conception of the invention in the United States on a date before 28 January 2003, which is the filing date of U.S. Patent Application Publication 2003/0222344 (Hosoyamada), and the inventors' diligence in constructively reducing to practice the invention conceived of before 28 January 2003.

We, Michael Kelly and Ravindhar K Kaw, hereby declare the following:

1) We are the sole inventors of the invention described and claimed in U.S. Patent Application, Serial No. 10/678,495, which was filed on 3 October 2003. Before 28 January 2003 and in the United States, we conceived an integrated circuit having at least the features of claims 4, 11 and 17, as amended in the response dated 19 October 2005, and at least features of claim 20, as presented in the response dated 19 October 2005.

2) Before 28 January 2003, we submitted to our corporate patent department, according to normal corporate procedures, an invention disclosure covering the conceived integrated circuit. Exhibit 1 includes copies of pages of the invention disclosure that we submitted before 28 January 2003. The copies included in Exhibit 1 are true and have had information redacted.

3) Exhibit 1 shows a diagram of an embodiment of an integrated circuit that corresponds to the embodiment of an integrated circuit shown in FIG. 2 (Exhibit 2) of the patent application. Specifically, the diagram in Exhibit 1 shows an integrated circuit comprising an integrated circuit package, a semiconductor substrate within the integrated circuit package, a plurality of wire bonds, and an interconnection substrate mounted on the semiconductor substrate.

4) Exhibit 1 shows expressly or impliedly each and every element of at least claim 4, as amended in the response dated 19 October 2005. Exhibit 1 shows an integrated circuit comprising an integrated circuit package having a first plurality of bonding pads; a semiconductor substrate within the integrated circuit package, including a circuit and a second plurality of bonding pads, and having a surface area; a plurality of wire bonds connecting selected ones of the first plurality of bonding pads to selected ones of the second plurality of bonding pads; and an interconnection substrate mounted on the semiconductor substrate, the interconnection substrate having a surface area smaller than the semiconductor substrate surface area and including only a conductive interconnect layer.

5) Exhibit 1 also shows expressly or impliedly each and every element of at least claim 11, as amended in the response dated 19 October 2005. Exhibit 1 shows an

integrated circuit as described in paragraph 4 of this declaration that includes the interconnection substrate flip chip mounted on the semiconductor substrate and the second plurality of bonding pads disposed within the peripheral areas.

6) Exhibit 1 also shows expressly or impliedly each and every element of at least claims 17, as amended in the response dated 19 October 2005, and claim 20 as presented in the response dated 19 October 2005. Exhibit 1 shows an integrated circuit comprising a semiconductor substrate including a circuit and a plurality of bonding pads, and having a surface area; and an interconnection substrate flip chip mounted on the semiconductor substrate, the interconnection substrate having a surface area smaller than the semiconductor substrate surface area and including only a conductive interconnect layer.

7) From before 28 January 2003 to 21 March 2003, the invention disclosure, which we submitted to our corporate patent department and which covered the conceived integrated circuit, was prepared for release to our patent attorney. On 21 March 2003, as shown in Exhibit 3, our corporate patent department sent our invention disclosure to our patent attorney. According to our patent attorney, Exhibit 3 is a true copy of correspondence between our corporate patent department and our patent attorney, and has had information redacted. On or about 15 May 2003, as shown in Exhibit 4, our patent attorney sent us a first draft of the patent application for our review. According to our patent attorney, Exhibit 4 is a true copy of correspondence between Michael Kelly and our patent attorney, and has had information redacted. We reviewed the first draft, and, as shown in Exhibit 5, on 2 July 2003 our patent attorney received our comments. According to our patent attorney, Exhibit 5 is a true copy of correspondence between Michael Kelly and our patent attorney, and has had information redacted. On 3 September 2003, as shown in Exhibit 6, our patent attorney provided the final draft of the application to our corporate patent department for approval. According to our patent attorney, Exhibit 6 is a true copy of correspondence between our patent attorney and our corporate patent department, and has had information redacted. Our patent attorney then filed the approved application on 03 October 2003.

8) We further declare that all statements made herein of our own knowledge are true; that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the

like, if so made, are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Ravindhar K. Kaw
Full Name of Inventor

USA
Citizenship

1128 MACHADO Ln. SAN JOSE, CALIF 95127
Residence

Ravindhar K Kaw
Inventor's Signature

Sept 8, 2006
Date

Michael Kelly
Full Name of Inventor

Citizenship

Residence

Inventor's Signature

Date

like, if so made, are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Ravindhar K. Kaw
Full Name of Inventor

Citizenship

Residence

Inventor's Signature

Date

Michael Kelly
Full Name of Inventor

USA
Citizenship

11221 S. 51st St., Phoenix, AZ 83424
Residence

Inventor's Signature

9/13/2006
Date

a "mini-substrate" interconnected to the top of an integrated circuit chip through the use of bumping (flip chip). This "mini-substrate" can be made of a single layer or multiple layers, using organic materials, ceramic or any other electrically conductive material like silicon, which can have metallic wires or planes printed in it to form an electrical interconnection to the integrated circuit.

Exhibit 1

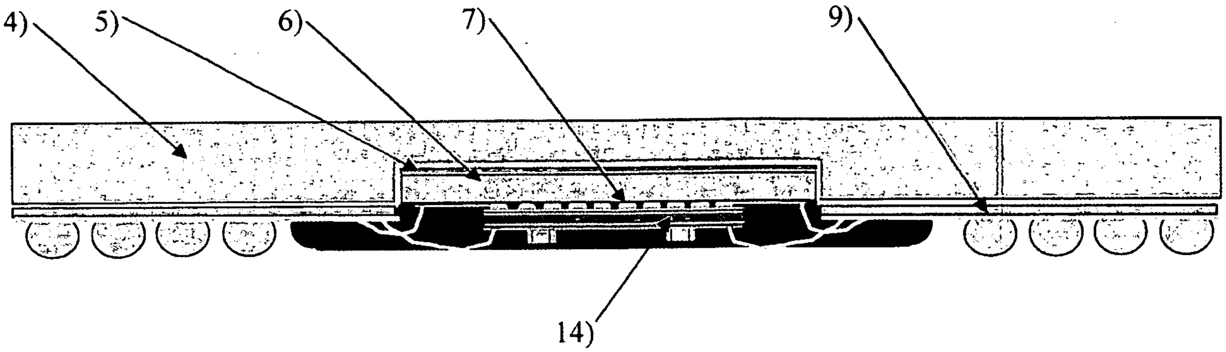

Figure 2

Referring to Figure 2, a typical cavity down configuration, a cavity down BGA package comprises a heat spreader (4), which adheres to a multiplayer package substrate (9). The integrated circuit (6) is attached to the heat spreader by the use of an adhesive (5).

Below the integrated circuit the mini substrate (14) is connected to the bottom surface of the integrated circuit with the small solder balls (or bumps) which can be an integral part of the mini substrate (7), or can be created on the wafer by standard bumping technology.

Portions of the circuitry of the integrated circuit is connected to the package substrate by normal wire bonding technology (15). The circuitry on the mini substrate is connected to the package substrate by wire bonds (12) or by circuitry designed specifically on the integrated circuit for this purpose (20).

Exhibit 1

Appln. No. 10/678,495
Amendment Dated 11/30/2004
Response to Office Action of Sept. 9, 2004
REPLACEMENT SHEET

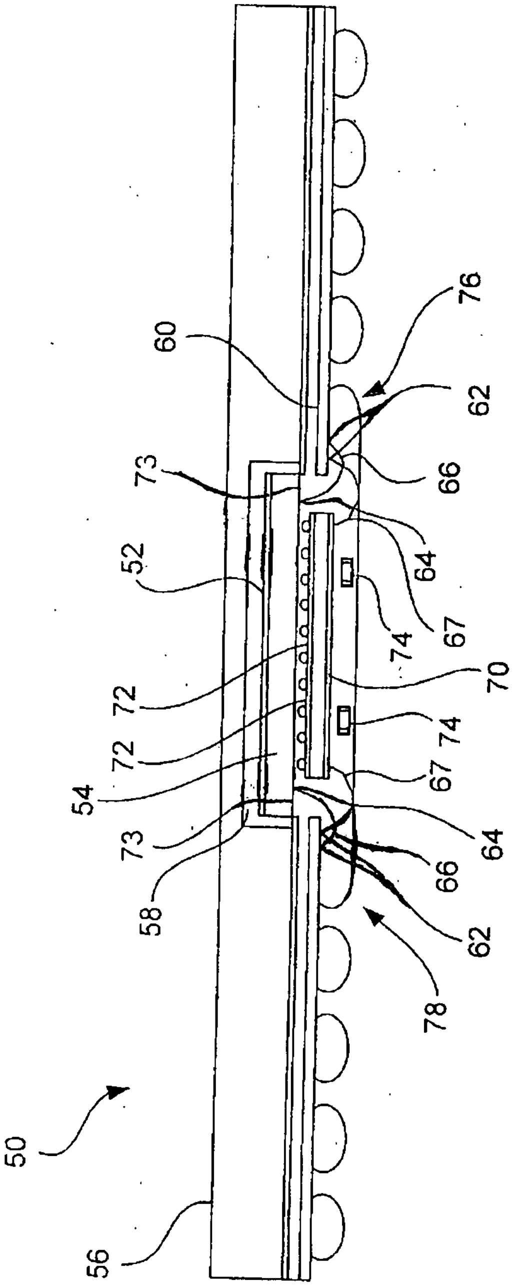

FIG. 2

Exhibit 2

From: patent_oc-manager@agilent.com
Sent: Friday, March 21, 2003 12:43 PM
To:
Cc:

Subject: RE: RFQ on 10030203-1 Application

Hi ,

Your not-to-exceed fee quotation of is approved and you are authorized to begin work immediately.

Exhibit 3

LAW OFFICES OF

GRAYBEAL JACKSON HALEY LLP

155 - 108TH AVENUE N.E., SUITE 350
BELLEVUE, WASHINGTON 98004-5973
TELEPHONE: (425) 455-5575
FACSIMILE: (425) 455-1046

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May 15, 2003

Mr. Michael G. Kelly
Agilent Technologies, Inc.
4238 SW Research Way
Corvallis, OR 97333

Re: United States Patent Application
For: **INTEGRATED CIRCUIT INCORPORATING FLIP CHIP AND WIRE BONDING**

Dear Mike:

Enclosed is a copy of the above-identified patent application for review If you or your coinventor (Ravindhar Kaw) have any changes for the description and/or drawings, please make the necessary revisions on the copy and return it to us for retyping.

Exhibit 4

Hi Richard,

I have made a few revisions, nothing too ~~mg~~ major.

Thanks,

Mike Kelly

RECEIVED
JUL 2 2003
GRAYBEAL JACKSON
HALEY LLP

Exhibit 5

From:
Sent: Wednesday, September 03, 2003 7:51 AM
To:
Cc:
Subject: 10030203-1

Hello! Attached is the above-referenced application and drawings for your review which has been approved by the inventors. Please let me know if you need anything further, and have a nice day.

10030203-1 Figures.pdf

10030203-1 patent app - 1st dr...

Exhibit 6